

New Low-Power 1.5-bit Time-Interleaved MDAC based on MOS Capacitor Amplification

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Abstract – In this paper a new time-interleaved 1.5-bit MDAC circuit is proposed. This circuit is well suited to be used in ultra low-power high-speed 4-to-8 bits pipeline ADCs. The required gain of two is implemented by switching a MOS capacitor from inversion into depletion within a clock-cycle. Low-power is achieved since no operational amplifiers are required but, instead, simple source-followers are used. Simulation results of a complete front-end stage of a 6-bit 2-channel pipeline ADC demonstrate the efficiency of the proposed technique.

I. INTRODUCTION

Next generation communications based on impulse radio Ultra-Wideband systems are targeted either for high data rate transfer or ultra-low power low data rate wireless sensor receivers [1]. In these applications, sampling-rates of the order of a few hundred mega-samples per second (MSPS) together with resolutions of about 6 bits are specified for the Analog-to-Digital Converters (ADCs) [2].

Pipeline ADCs can achieve very high-speeds with low power dissipation. However, their energy efficiency is much dependent on the optimum resolution-per-stage, on the scaling of the capacitance values and in the residue-amplifier topology used in the multiplying digital-to-analog converters (MDACs) of the pipeline stages. In closed-loop approaches, amplifiers with very high gain-bandwidth products have to be designed which dissipate a significant amount of power.

Parallel pipeline ADCs have been used to achieve medium resolutions at very high sampling rates [3, 4]. Also sharing some common blocks between two or more parallel ADCs, in a time-interleaved fashion can reduce the total power. The closed-loop multiply-by-two residue amplifiers usually integrated in the pipeline ADCs can be replaced by open-loop amplifiers [5, 6], reducing global size and power. However, it becomes mandatory to employ either digital gain-calibration [5] or employ replica circuits for implementing global-gain control techniques [7].

The work presented here, shows for the first time, a multiply-by-two residue amplifier (MBTA) implemented by switching a MOS capacitor from inversion into depletion within a clock-cycle (parametric amplification) using a new MOSCAP parametric amplifier configuration. A complete 2-channel interleaved 1.5-bit MDAC circuit based on this principle is described. This circuit is well suited for ultra low-power high-speed 4-to-8 bits pipeline ADCs. Moreover, low-

power is achieved since OPAMP based amplifiers are no longer required, and just simple source-followers are used for isolation between stages.

In section II, the principle of the parametric amplification capability of a MOS capacitor (MOSCAP) is shown. In section III, the new 2-channel 1.5-bit MDAC circuit is fully described. Section IV shows the simulation results and Section V draws the final conclusions.

II. LOW-GAIN AMPLIFICATION USING A MOS CAPACITOR

The needed MBTA in 1.5-bit stages of pipeline ADC can be achieved by using the parametric MOS amplification described in [8, 9] where a discrete-time amplifier was evaluated. In this amplifier, the gain is set through the reduction of the total equivalent gate capacitance of a single MOSCAP device, while maintaining the total gate charge between the sampling and the amplification phase. As explained in [8, 9], the capacitance reduction of a MOSCAP can be achieved by moving it from inversion into depletion, as result of changing the control voltage ($V_{control}$) applied to the drain from the lower power supply voltage (V_{SS}) to the positive power supply (V_{DD}), as shown in Figs.1 (a) and (b).

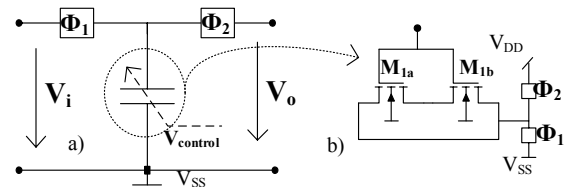


Figure 1. (a) MOSCAP parametric amplifier; (b) MOSCAP implementation using 2 separated devices.

The amplifier circuit operates as follows. During phase Φ_1 the input signal is sampled by M_{1a} - M_{1b} and a corresponding charge is stored. Considering that, in Φ_2 both gate charges remain constant (gates are floating), the gate voltage will change by a gain of, approximately, $v_o/v_i = C_{ox}/C_{gb}$, where C_{ox} is the total gate-oxide capacitance and C_{gb} is the gate-bulk capacitance during the amplification phase [9].

The main differences of the basic MOSCAP structure used here from the one used in [8, 9] lies on the fact that 2 half-sized MOSCAPs are used instead of a single one and, on the other hand, their short-circuited sources are left floating.

The main advantage of this structure is that it decreases the total gate capacitance during the amplification phase since half of the value is left floating. Hence, the total loading capacitance in Φ_2 is reduced by half, and amplification gains above 3 can now be easily achieved with an nMOS-type MOSCAP (nMOSCAP) which is of paramount importance to allow the practical implementation of an overall gain of 2 for a complete MDAC. A simulation of the obtainable gain is shown in Fig. 2 by electrical simulations of the circuit shown in Fig. 1.

Figure 2. Parametric amplifier gain as a function of the input DC level.

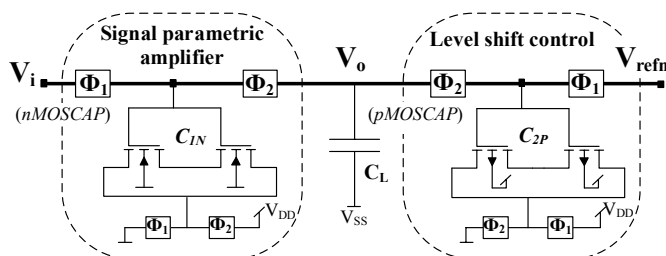


Figure 3. CMOS discrete-time amplifier with output level shift control.

$$V_O \approx \frac{\alpha_{C1n}}{k} V_i + \frac{\alpha_2 - \alpha_4}{k} V_{DD} + \frac{\alpha_4}{k} V_{refn} + \frac{\alpha_3}{k} V_{CL,\phi1} \quad (1)$$

Parameter k models the gain reduction due to the load capacitance C_L and C_{2P} during phase Φ_2 . Parameter α_{CIN} reflects the capacitance variation from phase Φ_1 to phase Φ_2 for C_{IN} . Parameter α_2 represents the relation between C_{2P} , during phase Φ_2 , and C_{IN} in phase Φ_1 . The remaining parameters α_3 and α_4 describe the ratio of C_L and C_{2P} in phase Φ_2 with respect to the value of C_{IN} during phase Φ_2 .

III. 1.5-BIT 2-CHANNEL MDAC ARCHITECTURE AND DESIGN

A complete 2-channel time-interleaved 1.5-bit pipeline stage is shown in Fig. 4 where, for simulation purposes, an ideal 1.5-bit quantizer (1.5-bit sub-ADC) is used. The proposed 1.5-bit 2-channel MDAC comprises two fully-differential MDACs (1 and 2) made of four single-ended MDACs (versions p (Fig. 5) and n named half-MDAC, respectively for the positive and negative signal paths) and two source-follower circuits. As stated before, these buffers are required to isolate the loading effect of the next pipeline stage.

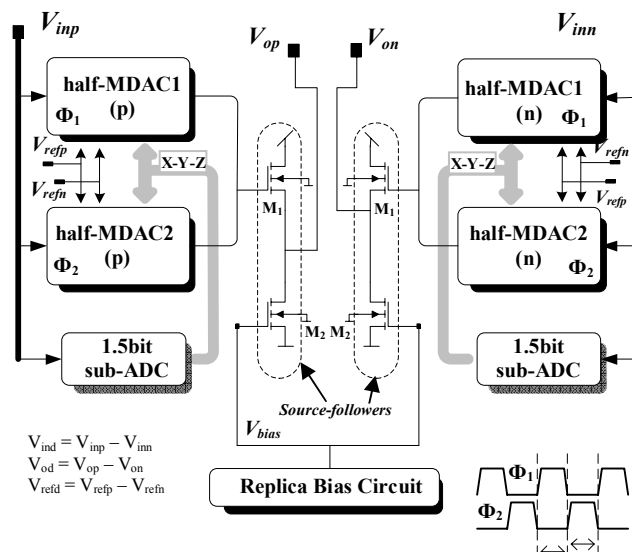


Figure 4. Two-channel time-interleaved 1.5-bit pipeline stage comprising two fully-differential 1.5-bit MDACs.

The schematic of each 1.5-bit half-MDAC circuit is shown in Fig. 5 (in this case the p-type version is shown). Three switched MOSCAPs, C_X , C_Y and C_Z , always operating in inversion have been added. The addition and subtraction function of the 1.5-bit MDAC depends on the values of the 3-bit X, Y, Z code (only one bit is enabled in each conversion cycle), which is provided by the 1.5-bit sub-ADC.

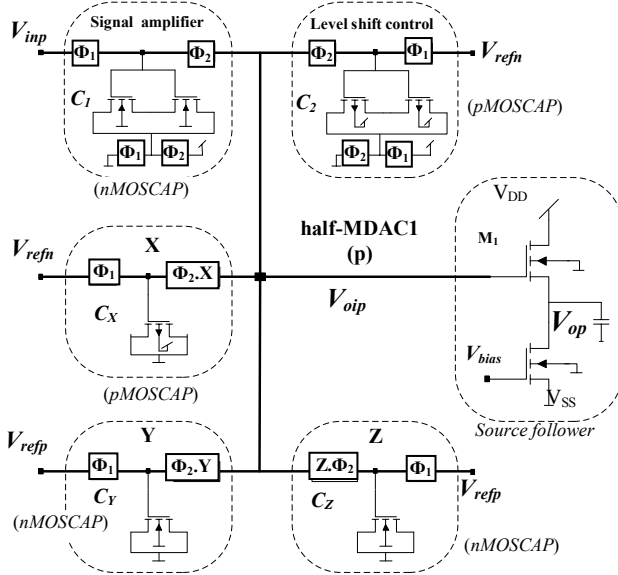


Figure 5. Internal 1.5bit half-MDAC single-ended circuit (p version).

During phase Φ_1 , the input signal is sampled by C_1 , the negative reference voltage (V_{refn}) is sampled by C_2 and by C_X and the positive reference voltage (V_{refp}) is sampled by C_Y and by C_Z . In the residue-amplification phase Φ_2 , the capacitance values of C_1 and C_2 decrease due to the change from inversion into depletion region, but the capacitance values C_X , C_Y and C_Z remain unchanged. Depending on the value of the X, Y, Z code provided by the 1.5-bit sub-ADC block, during phase Φ_2 , only one of the capacitances C_X , C_Y or C_Z is selected to be connected to the input of the corresponding source-follower for charge re-distribution.

Applying, to this half-MDAC, the same methodology used for the parametric amplifier transfer function, results in a similar equation to (1) where new terms are added to take into account the charge re-distribution of C_X , C_Y and C_Z . Additionally the k factor also includes the contribution of these MOSCAPs. Considering the differential MDAC implementation, the common-mode components present in (1) are removed, resulting in a final expression for the differential voltage, V_{od} , at the inputs of the source-followers given by:

$$V_{od} \approx \frac{g_{m1}}{g_{m1} + g_{sb1}} \cdot \left(\frac{\alpha_{C1n}}{k} V_{id} - k_{DAC} V_{refd} \cdot X + k_{DAC} V_{refp} \cdot Y + 0 \cdot Z \right) \quad (2)$$

where $C_{1,\phi1} = \alpha_{C1} \cdot C_{1,\phi2}$, $C_{2,\phi2} = \alpha_2 \cdot C_{1,\phi2}$, $C_L = \alpha_3 \cdot C_{1,\phi2}$, $C_{2,\phi1} = \alpha_4 \cdot C_{1,\phi2}$, $C_{XYZ} = \alpha_5 \cdot C_{1,\phi2}$, $k = 1 + \alpha_2 + \alpha_3 + \alpha_5$ and $k_{DAC} = C_{XYZ} / (C_{1,\phi2} \cdot k)$. Transconductances g_{m1} and g_{sb1} represent, respectively, the main and body-effect transconductances of the main device of the source-follower (M_1).

In (2), it has been assumed that both half-MDAC have equally sized transistors and C_X , C_Y and C_Z are all nominally equal to C_{XYZ} . A differential MDAC is then composed by two equal size half-MDACs, in which only X and Y signals exchange to implement the n-type version.

Note that, due to the body-effect of the source-followers, their gain is smaller than one. Hence, to compensate this effect the complete 1.5-bit half-MDACs are adjusted and sized to have a gain factor exactly equal to two.

B) Replica-bias circuit output common-mode control

Another important aspect is that the output common-mode voltage (VCMO) at the outputs of the source-followers can not vary too much in order to avoid DC accumulation errors in the subsequent pipeline stages. A replica-bias circuit as the one depicted in Fig. 6 is used to guarantee that VCMO is restored at the output of every 1.5-bit MDAC and adjusted to a proper value against process and supply variations. Note that a single replica-bias block can be used to bias all MDACs in the pipeline chain. It comprises two time-interleaved half-MDACs connected to a same replica source-follower. The average voltage at the buffer output is set and controlled by a negative feedback loop which includes a very simple amplifier. The objective is to replicate the operation of the differential MDAC and controlling the common mode voltage present at the MDACs buffers outputs through a biasing voltage V_{bias} . As referred before, stabilizing the output common-mode component at the outputs of each stage prevents biasing error propagation along the pipeline. Note that the OTA used here does not need a high bandwidth since it is not inserted in the main signal path. Therefore it can be designed with minimum current.

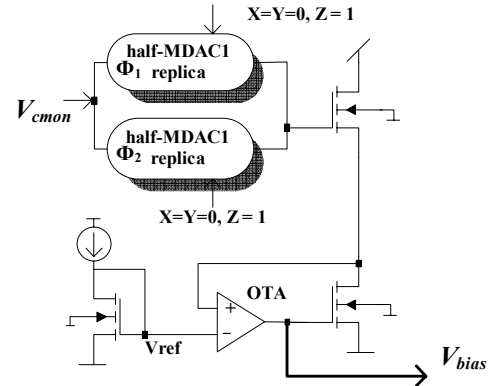


Figure 6. Replica bias block used to generate V_{bias} for all source-followers.

IV. SIMULATION RESULTS

A fully-differential time-interleaved 1.5-bit MDAC has been designed in 130nm 1P-8M CMOS technology for a 1.2V supply voltage. This MDAC was specially designed to meet the specifications of a front-end stage for a 2-channel 6-bit 250 MS/s pipeline ADC. The adopted differential full-scale input is 400 mVp-p and, to reduce the size of the switches, 1.0 V and 0.0 V are used for V_{refp} and V_{refn} , respectively. The input and output common-mode-voltages are set to 0.65 V and 0.45 V, respectively.

For the switches connected to the input signals, asymmetrical CMOS transmission gates with dummy structures are used to minimize signal-dependent charge injection. All remaining switches are made only of single nMOS or pMOS devices. Very small source-followers are used with an input parasitic capacitance smaller than 50 fF and with a driving capability of a fixed load of 500 fF.

Capacitors C_{IN} , C_{2P} and C_{XYZ} are sized to have, in inversion, a capacitance value of about 600 fF, 200 fF and 200 fF, respectively. These values are then fine-tuned by exhaustive simulations in order to obtain a precise gain of 2.0 in typical conditions and when Z is active. A channel length of 360 nm is used in all MOSCAPs to achieve low transition times when switching the MOSCAPs from inversion into depletion region (and vice-versa).

Fig. 7 (a), (b) and (c) show the simulated conversion characteristic of the 1.5-bit MDAC for a slow differential input ramp signal and for 3 different process corners. A slow input ramp signal was used to obtain accurate simulations results but the 1.5-bit MDAC is working at full speed (250 MS/s). Simulated gain error variation at the output is smaller than 3.2% (0.4 % of error in typical conditions and when Z is active) for all 3 corners. The complete 2-channel 1.5-bit MDAC core dissipates only 2.37 mW when operating at 250 MS/s and at 1.2 V. The replica bias block dissipates 0.73 mW and the two source-followers dissipate only 0.49 mW.

V. CONCLUSIONS

In this paper a new time-interleaved 1.5-bit MDAC circuit was proposed. This circuit is well suited for ultra low-power high-speed 4-to-8 bits pipeline ADCs. The gain of two was implemented by switching a MOS capacitor from inversion into depletion within a clock-cycle using a new MOSCAP configuration. Low-power was achieved since no operational amplifiers are required but, instead, simple source-followers are used. Simulation results of a complete front-end stage of a 6-bit 2-channel pipeline ADC demonstrated the efficiency of the proposed technique.

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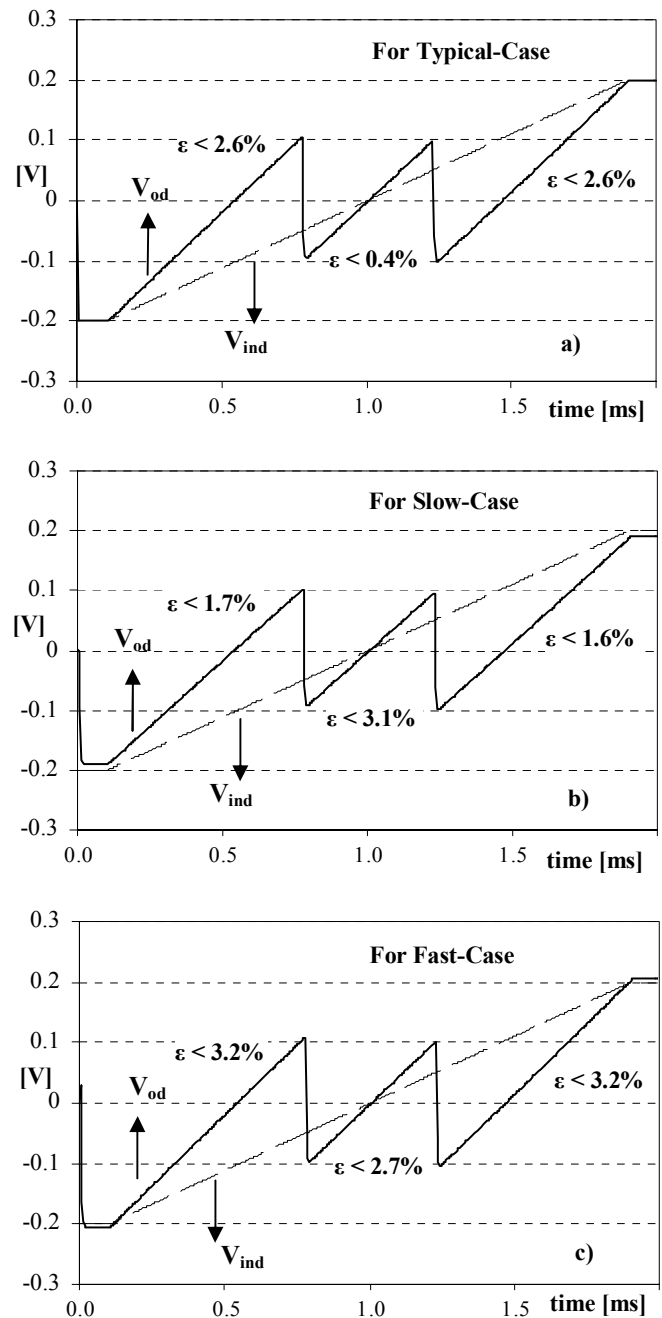


Figure 7: Simulations of the differential output of a 2-channel 1.5-bit MDAC for a differential input ramp signal: a) typical; b) Slow-case; c) Fast-case;